



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,884	04/17/2001	Kevin L. Denis	H-303	5188

26245 7590 07/29/2003

DAVID J COLE
E INK CORPORATION
733 CONCORD AVE
CAMBRIDGE, MA 02138-1002

EXAMINER

NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
----------	--------------

2823

DATE MAILED: 07/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/836,884

Applicant(s)

DENIS ET AL.

Examiner

Khiem D Nguyen

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 April 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 April 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

Art Unit: 2823

DETAILED ACTION

Response to Amendment

Response to Applicant's Arguments

Applicant's arguments filed 04-28-2003 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi (U.S. Patent 6,461,901) in view of Derwent Abstract (JP 63084089).

Noguchi teaches a process for forming at least one transistor on a substrate 100, the process comprises depositing on the substrate at least one layer of semiconductor material (amorphous silicon) 104 by plasma enhanced chemical vapor deposition wherein the semiconductor material is affected on a continuous web of substrate (col. 10, lines 9-40 and FIGS. 10A-C). The process further comprising:

depositing a metal layer (chromium (Cr)) 102 upon the substrate on the same side thereof as the semiconductor material wherein the metal layer is deposited as a continuous film and is thereafter patterned prior to deposition of the semiconductor material thereon (col. 15, lines 46-51);

Art Unit: 2823

depositing a dielectric layer (silicon nitride) 103 over the metal layer by plasma enhanced chemical vapor deposition prior to the deposition of the semiconductor layer; and,

depositing a n-type silicon layer 105 over the amorphous silicon layer where in a patterned layer of metal 107 has walls defining apertures extending through the metal layer is thereafter formed over the n-type silicon, and the resultant structure is thereafter etched to remove portions of the n-type silicon not covered by the patterned layer of metal.

Noguchi discloses in FIG. 1 that the amorphous silicon 1104 is not patterned so that it extends continuously between at least some pairs of adjacent transistors as recited in present claim 20 by the applicants.

Noguchi also discloses in (col. 22, lines 14-43) wherein the deposition of the semiconductor material is effected at a temperature in excess of about 300°C as recited in present claim 13 by the applicants.

Noguchi fails to teach that the substrate comprises a polyphenylene polyimide wherein the polyphenylene polyimide is a derivative of biphenyl-3,3', 4,4'-tetracarboxylic acid and wherein the substrate is heated to a temperature greater than about 150°C for a period of at least about 1 minute or to a temperature greater than about 250°C for a period of at least 1 hour before deposition of the passivating layer and wherein the substrate is heated to a temperature greater than about 250°C for a period of at least about 5 hours after deposition of the passivating layer as recited in present claims 1-3, 8-10.

(JP 63084089) teaches producing a substrate comprises 3,3', 4,4' biphenyl tetracarboxylic acid wherein the substrate is heated to a temperature from 100°C-300°C in at least 0.5 hour before the deposition of any other layer thereto (See the Abstract). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate (JP 63084089)'s teaching into Noguchi's method because in doing so a substrate has excellent heat resistance, cold resistance, mechanical property, electric property, wear resistance, chemical resistance and curling resistance can be obtained (See the Abstract).

Noguchi fails to teach wherein a passivating layer comprises silicon dioxide or aluminum nitride having a thickness in the range of about 20 to about 100 nm is deposited on both surfaces of the substrate before the semiconductor material is deposited thereon as recited in present claims 4-7. However, it is well-known to one of ordinary skill in the art of making semiconductor devices to deposit a passivating layer comprises silicon dioxide or aluminum nitride having a desired thickness on both surfaces of the substrate before the semiconductor material is deposited thereon.

Noguchi teaches that the substrate is being heated for the time duration but fails to teach the ranges for the time duration as recited in present claims 8-10. However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for the time duration through routine experimentation and optimization to obtain optimal or desired device performance because the time duration is result-effective variables and there is no evidence indicating that the time duration is critical and it has been held that it is not inventive to discover the

Art Unit: 2823

optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Response to Amendment

Response to Applicant's Arguments

Applicant's arguments filed 04-28-2003 have been fully considered but they are not persuasive.

In response to Applicant's argument that Noguchi forms his thin film transistors on quartz glass instead of on a polyphenylene polyimide substrate as recited by the applicants, examiner disagree, the primary reference (Noguchi U.S. Patent 6,461,901) discloses a process for forming at least one transistor on a substrate (col. 10, lines 9-40 and FIGS. 10A-C) but fails to explicitly disclose wherein the substrate comprises a polyphenylene polyimide as recited by the applicants in claim 1 (line 3), the secondary reference (Derwent Abstract JP 63084089) recognized that substrate comprises polyphenylene polyimide has excellent heat resistance, cold resistance, mechanical property, electric property, wear resistance, chemical resistance and curling resistance (Abstract). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate (Derwent Abstract JP 63084089)'s teaching into Noguchi's method to form the transistors on a polyphenylene polyimide substrate to obtain the benefits as taught by the Derwent Abstract.

In response to Applicant's argument that Neither Noguchi nor the Abstract disclose the use of a metal layer having apertures extending therethrough as recited in present claim 12, examiner disagree, Noguchi disclose the substrate (FIG. 10B, 100)

Art Unit: 2823

comprises a metal layer (FIG. 10B, 107) wherein the metal layer has walls defining apertures extending through the metal layer (col. 10, lines 9-40 and FIGS. 10A-C).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Art Unit: 2823

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
July 21, 2003



Chik Chik
Supervisory Patent Examiner
Technology Center 2800